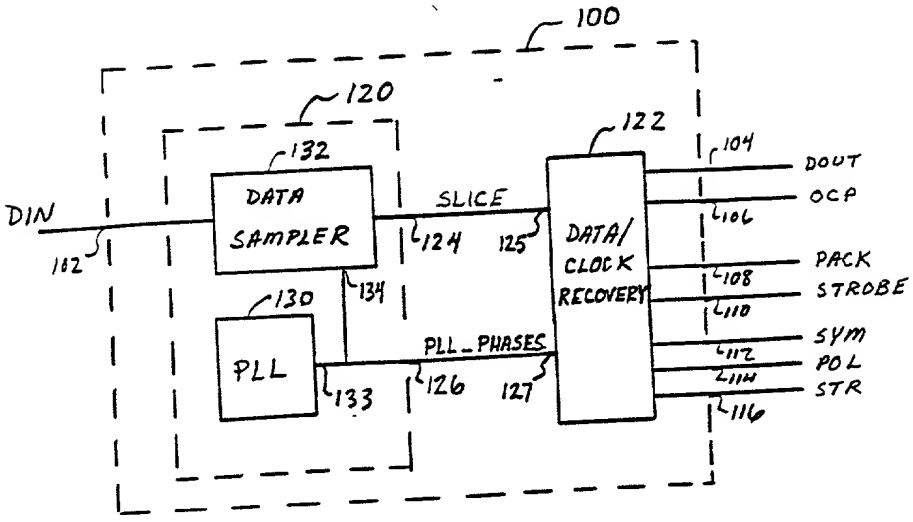
100
120
122
132
DATA SAMPLER
SLICE
DIN
102
124
125
DATA/ CLOCK RECOVERY
104
DOUT
OCP
106
PACK
108
STROBE
110
SYM
112
POL
114
STR
116
130
PLL
134
PLL_PHASES
133
126
127

FIG. 1

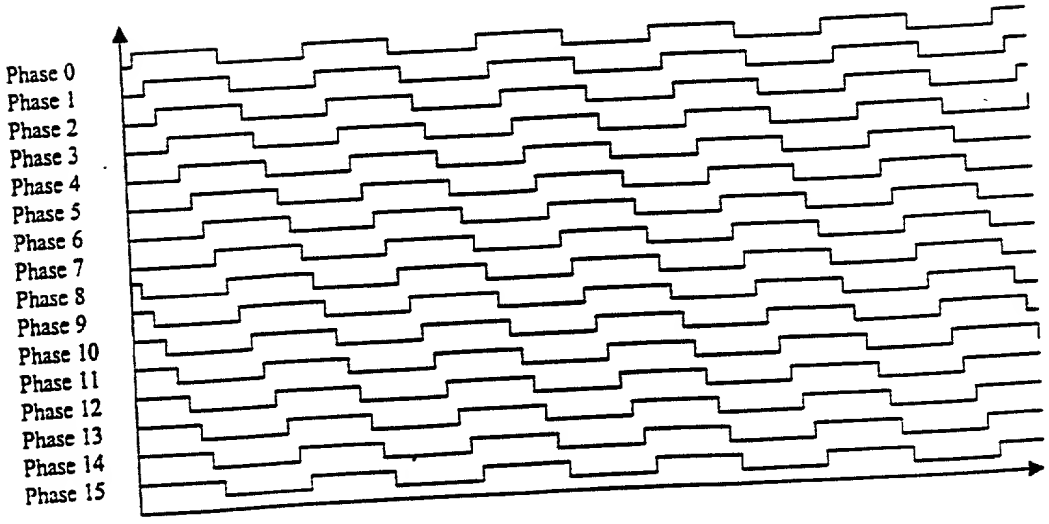
Phase 0
Phase 1
Phase 2
Phase 3
Phase 4
Phase 5
Phase 6
Phase 7
Phase 8
Phase 9
Phase 10
Phase 11
Phase 12
Phase 13
Phase 14
Phase 15

FIG. 2

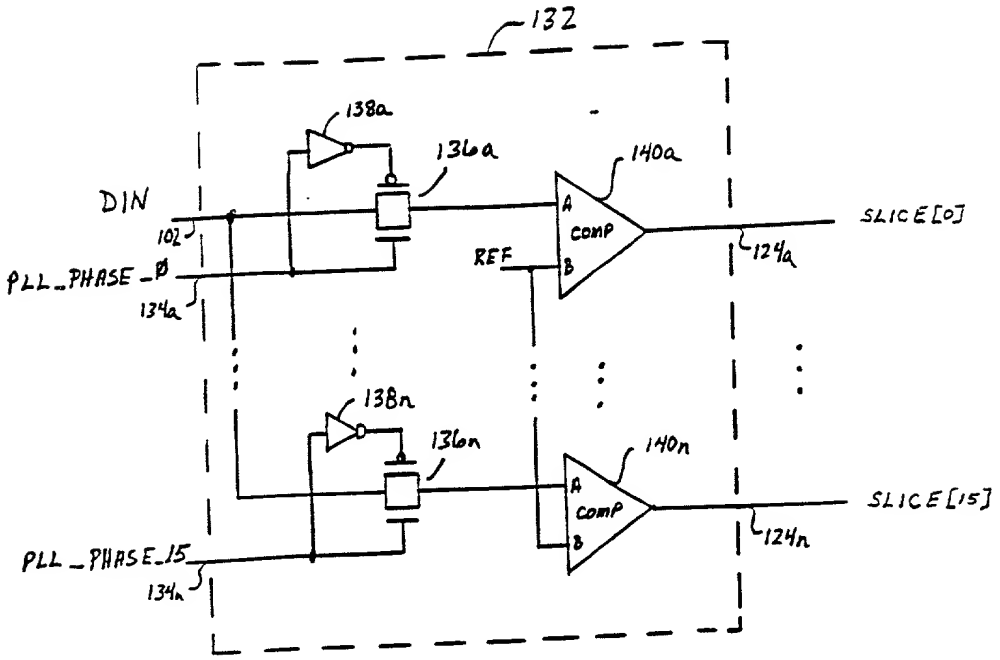
132
138a
136a
140a
DIN
102
A
COMP
B
SLICE[0]
REF
PLL_PHASE_Ø
134a
124a
138n
136n
140n
SLICE[15]
PLL_PHASE_15
134n
124n

FIG. 3

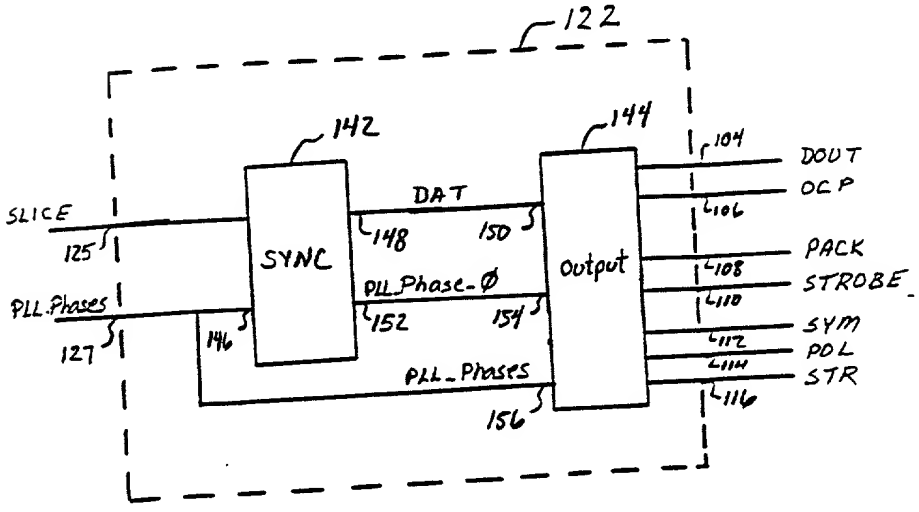
122
142
144
SLICE
125
SYNC
DAT
148
150
Output
104
DOUT
OCP
106
PACK
108
STROBE
110
SYM
112
POL
114
STR
116
PLL_Phases
127
146
PLL_Phase_Ø
152
154
PLL_Phases
156

FIG. 4

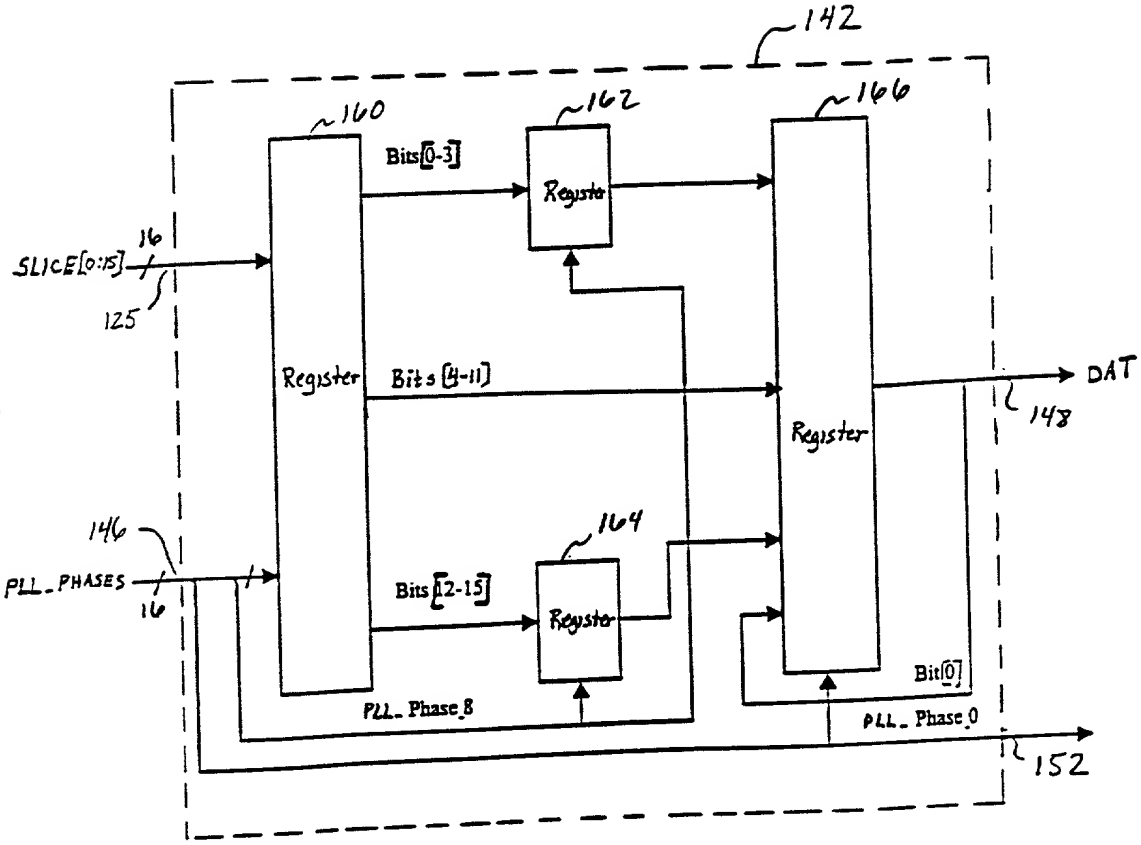
142
160
162
166
Bits[0-3]
Register
SLICE[0:15]
16
125
Register
Bits[4-11]
Register
DAT
148
146
164
PLL_PHASES
16
Bits[12-15]
Register
Bit[0]
PLL_Phase_8
PLL_Phase_0
152

FIG. 5

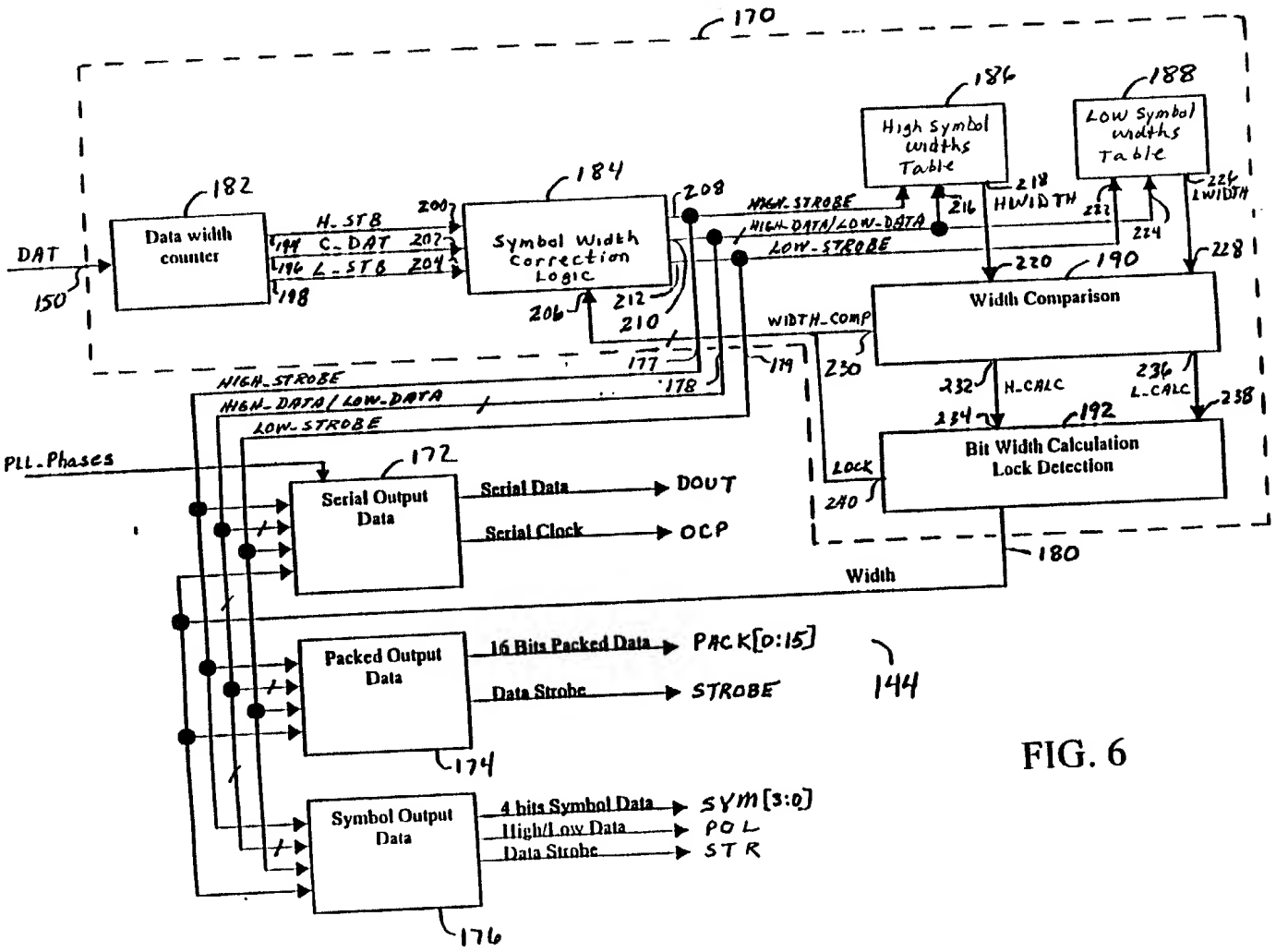

FIG. 6

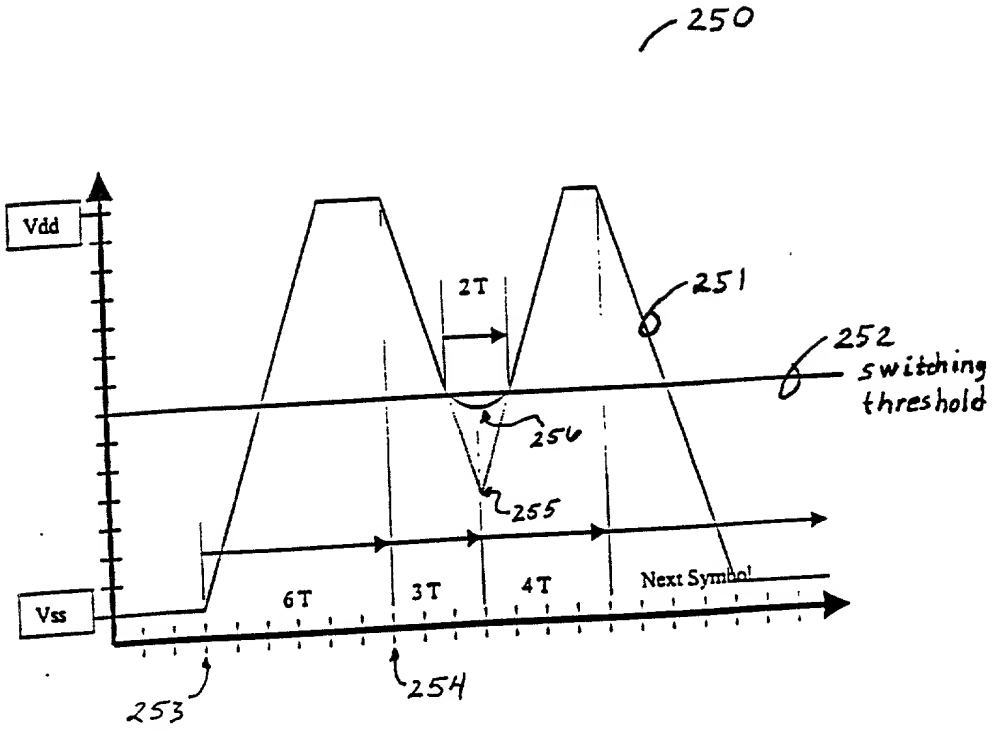
250
Vdd
Vss
2T
251
252
switching
threshold
256
255
6T
3T
4T
Next Symbol
253
254

FIG. 7

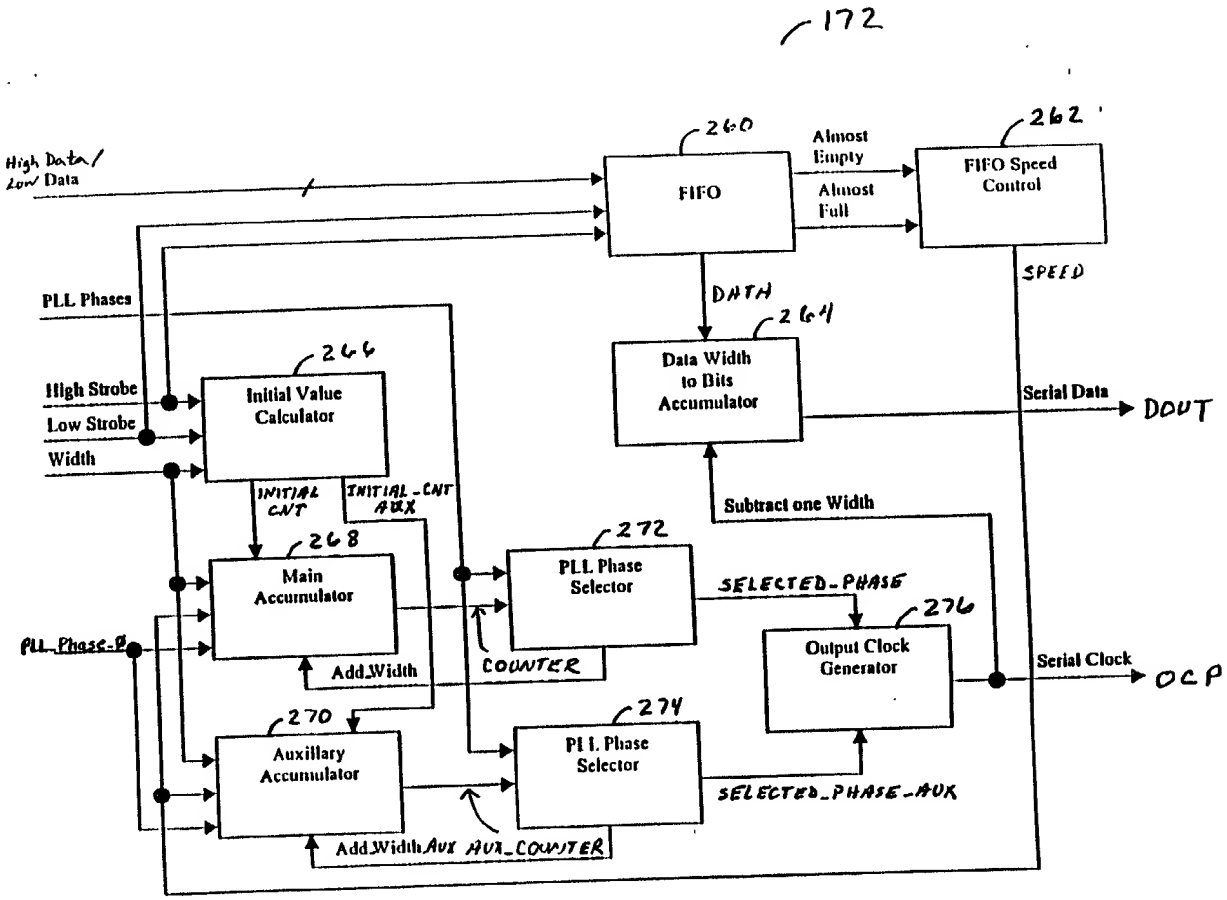

FIG. 8

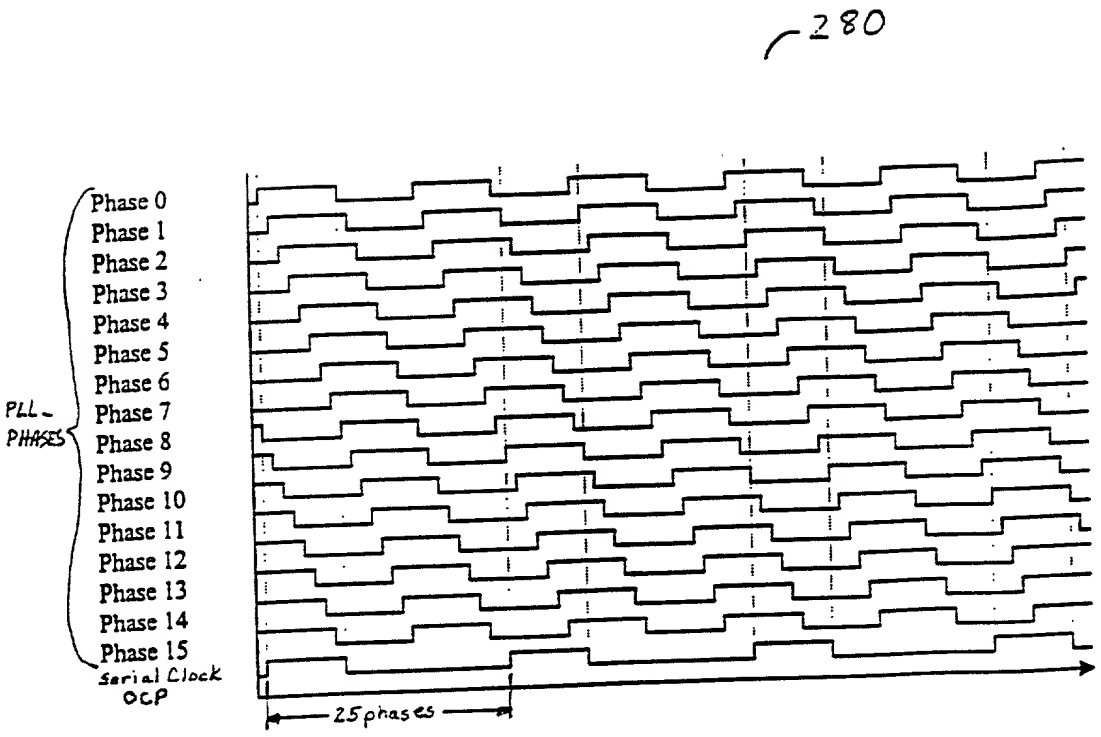
280
Phase 0
Phase 1
Phase 2
Phase 3
Phase 4
Phase 5
Phase 6
Phase 7
Phase 8
Phase 9
Phase 10
Phase 11
Phase 12
Phase 13
Phase 14
Phase 15
PLL PHASES
Serial Clock OCP
25 phases

FIG. 9

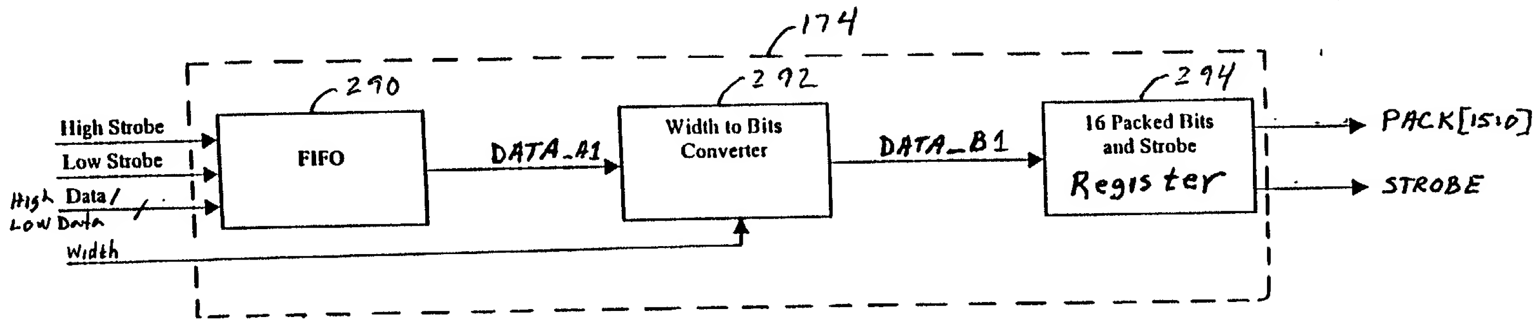
174
290
292
294
High Strobe
Low Strobe
High Data / Low Data
Width
FIFO
DATA_A1
Width to Bits Converter
DATA_B1
16 Packed Bits and Strobe Register
PACK[15:0]
STROBE

FIG. 10

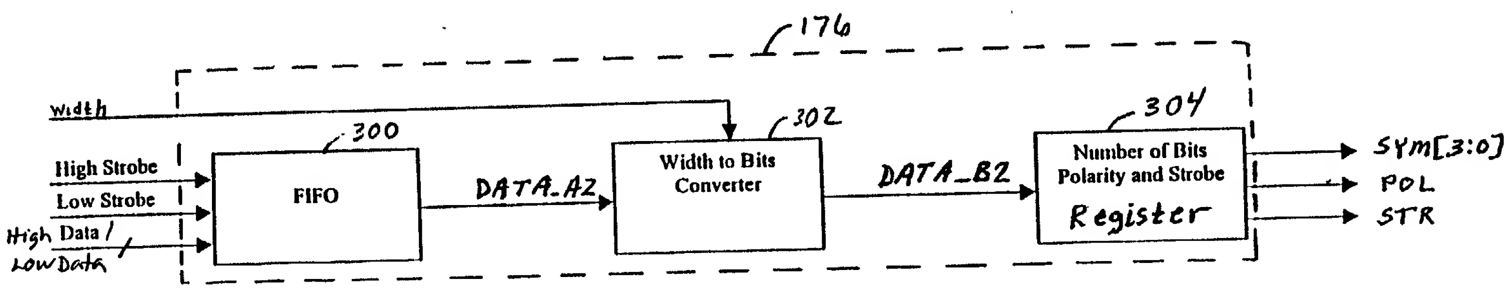
176
300
302
304
Width
High Strobe
Low Strobe
High Data / Low Data
FIFO
DATA_A2
Width to Bits Converter
DATA_B2
Number of Bits Polarity and Strobe Register
SYM[3:0]
POL
STR

FIG. 11

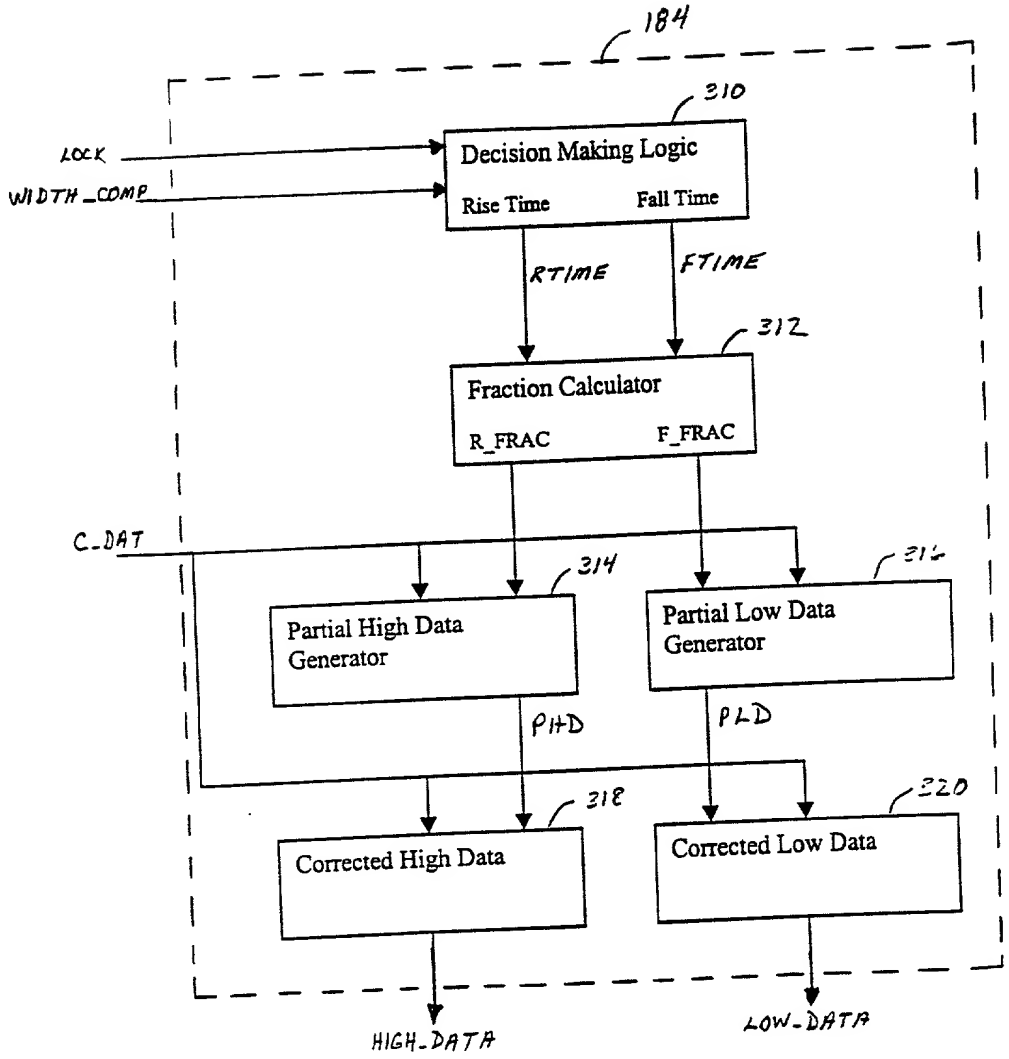
184
310
LOCK
WIDTH_COMP
Decision Making Logic
Rise Time
Fall Time
RTIME
FTIME
312
Fraction Calculator
R_FRAC
F_FRAC
C_DAT
314
Partial High Data Generator
316
Partial Low Data Generator
PHD
PLD
318
Corrected High Data
320
Corrected Low Data
HIGH_DATA
LOW_DATA

FIG. 12

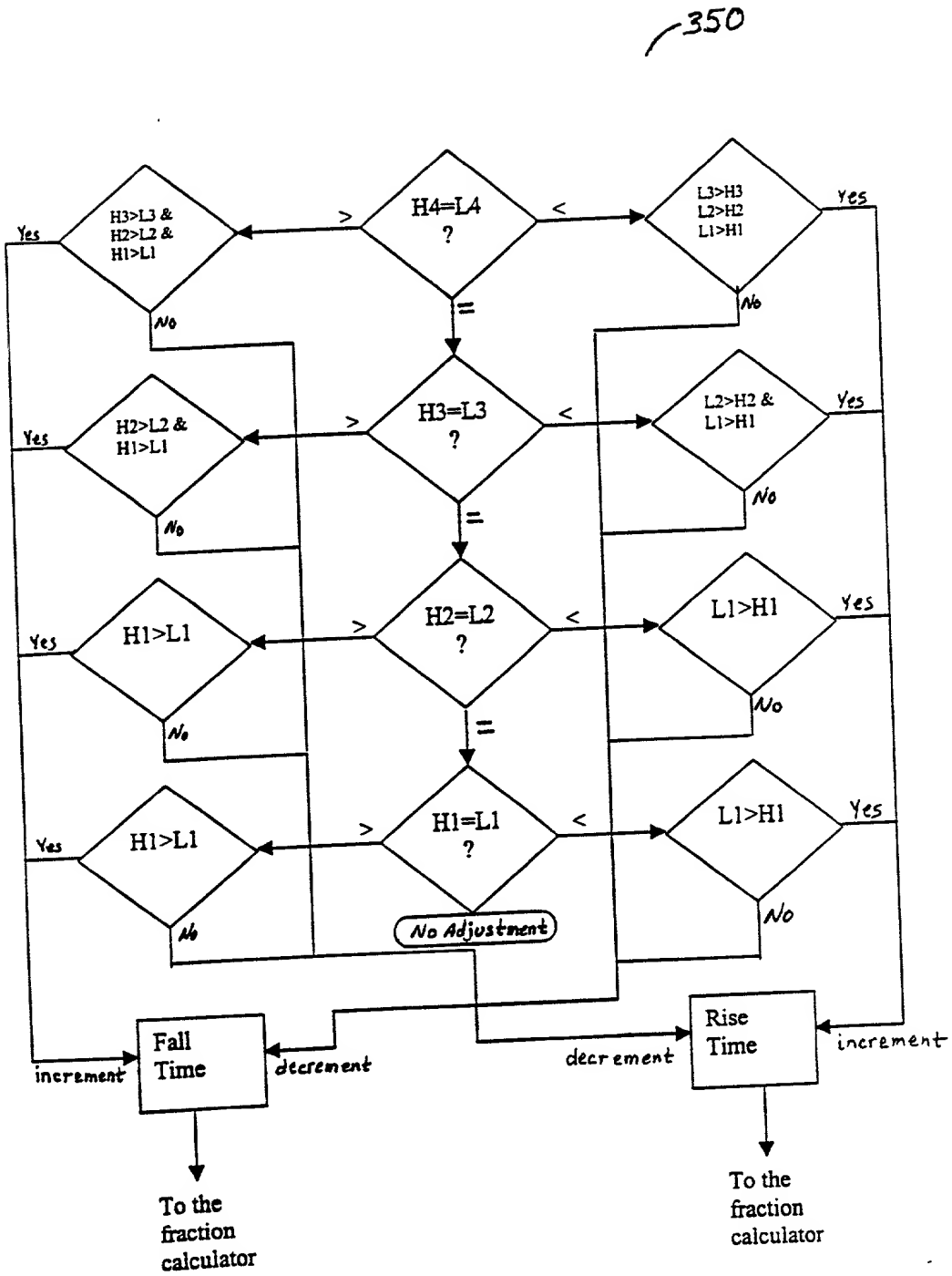
350
H4=L4 ?
H3>L3 & H2>L2 & H1>L1
L3>H3 L2>H2 L1>H1
H3=L3 ?
H2>L2 & H1>L1
L2>H2 & L1>H1
H2=L2 ?
H1>L1
L1>H1
H1=L1 ?
H1>L1
L1>H1
Yes
No
>
<
=
No Adjustment
Fall Time
Rise Time
increment
decrement
decrement
increment
To the fraction calculator
To the fraction calculator

FIG. 13

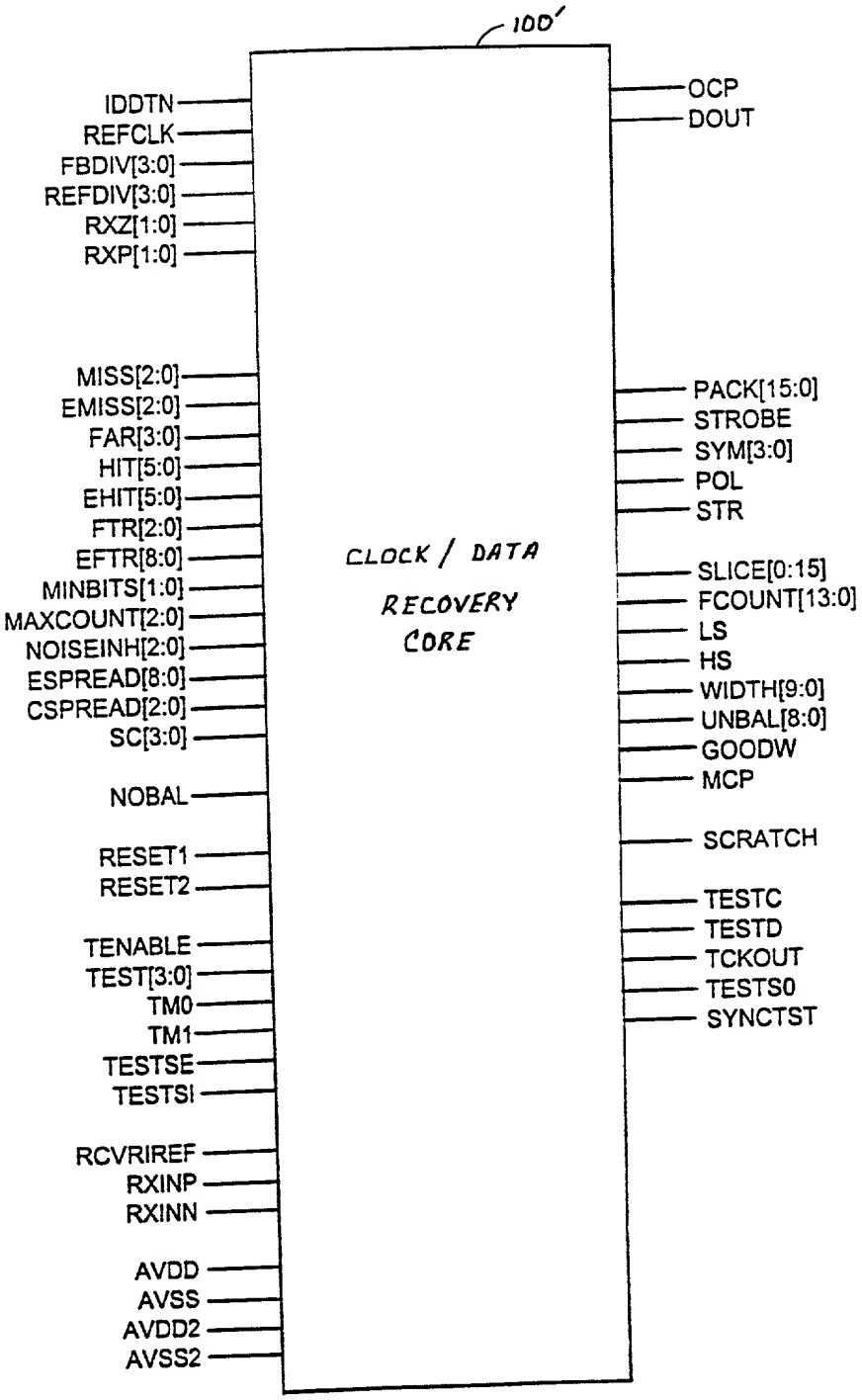
100'
IDDTN
REFCLK
FBDIV[3:0]
REFDIV[3:0]
RXZ[1:0]
RXP[1:0]
MISS[2:0]
EMISS[2:0]
FAR[3:0]
HIT[5:0]
EHIT[5:0]
FTR[2:0]
EFTR[8:0]
MINBITS[1:0]
MAXCOUNT[2:0]
NOISEINH[2:0]
ESPREAD[8:0]
CSPREAD[2:0]
SC[3:0]
NOBAL
RESET1
RESET2
TENABLE
TEST[3:0]
TM0
TM1
TESTSE
TESTSI
RCVRIREF
RXINP
RXINN
AVDD
AVSS
AVDD2
AVSS2
CLOCK / DATA
RECOVERY
CORE
OCP
DOUT
PACK[15:0]
STROBE
SYM[3:0]
POL
STR
SLICE[0:15]
FCOUNT[13:0]
LS
HS
WIDTH[9:0]
UNBAL[8:0]
GOODW
MCP
SCRATCH
TESTC
TESTD
TCKOUT
TESTS0
SYNCTST

FIG. 14

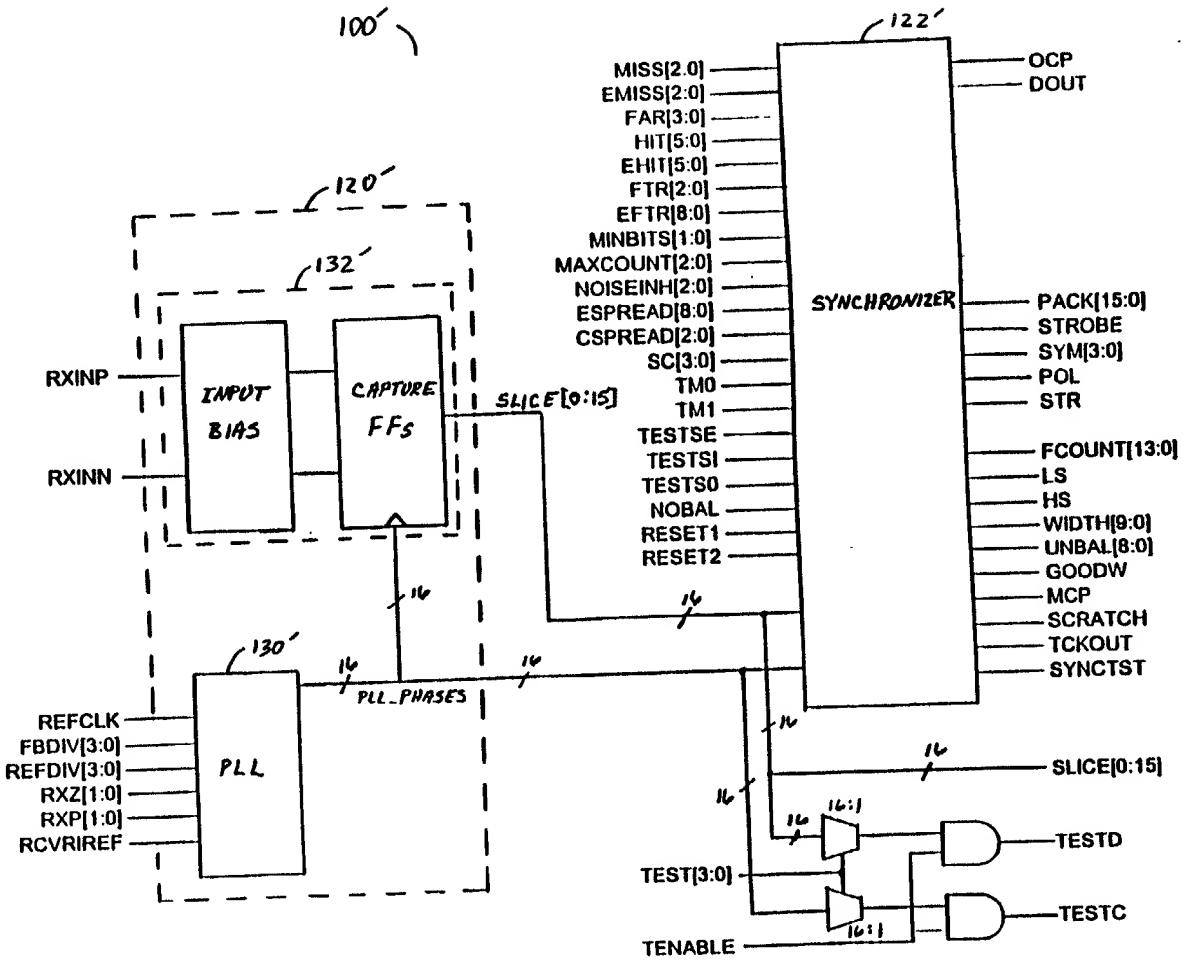
100'
122'
120'
132'
130'
MISS[2:0]
EMISS[2:0]
FAR[3:0]
HIT[5:0]
EHIT[5:0]
FTR[2:0]
EFTR[8:0]
MINBITS[1:0]
MAXCOUNT[2:0]
NOISEINH[2:0]
ESPREAD[8:0]
CSPREAD[2:0]
SC[3:0]
TM0
TM1
TESTSE
TESTSI
TESTS0
NOBAL
RESET1
RESET2
SYNCHRONIZER
OCP
DOUT
PACK[15:0]
STROBE
SYM[3:0]
POL
STR
FCOUNT[13:0]
LS
HS
WIDTH[9:0]
UNBAL[8:0]
GOODW
MCP
SCRATCH
TCKOUT
SYNCTST
RXINP
RXINN
INPUT BIAS
CAPTURE FFs
SLICE[0:15]
PLL_PHASES
REFCLK
FBDIV[3:0]
REFDIV[3:0]
RXZ[1:0]
RXP[1:0]
RCVRIREF
PLL
16:1
TEST[3:0]
TENABLE
TESTD
TESTC
16

FIG. 15

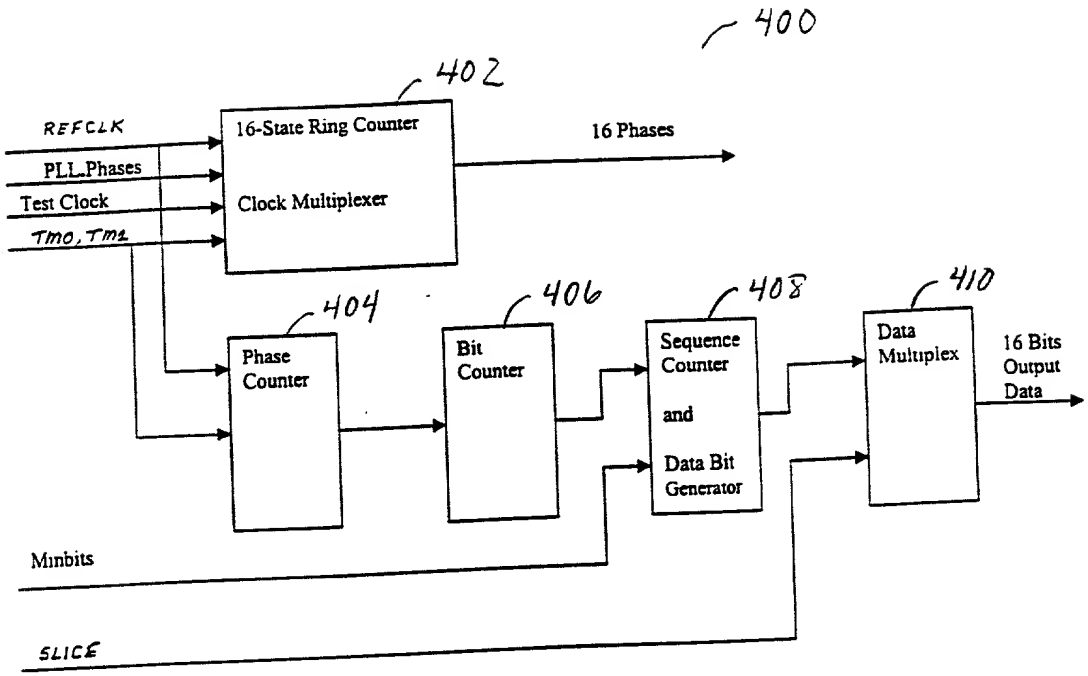
400
402
REFCLK
PLL_Phases
Test Clock
TM0, TM1
16-State Ring Counter
Clock Multiplexer
16 Phases
404
Phase Counter
406
Bit Counter
408
Sequence Counter
and
Data Bit Generator
410
Data Multiplex
16 Bits Output Data
Minbits
SLICE

FIG. 16

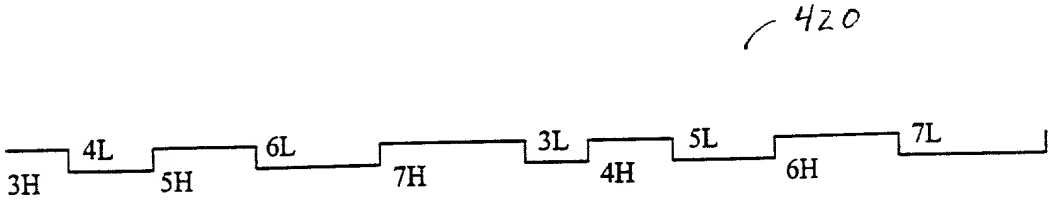
420
3H
4L
5H
6L
7H
3L
4H
5L
6H
7L

FIG. 17